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Date Mailed : December 4, 2006
Serial No. :10/777,128
Patent No. :7,109,544 B2
Patent Issued :September 19, 2006
Title :ARCHITECTURE VERTICAL TRANSISTOR CELLS AND TRANSISTOR-CONTROLLED MEMOR CELLS

Re: Request for Certificate of Correction

Consideration has been given your request for the issuance of a certificate of correction for the above-identified patent.

Respecting the alleged errors noted in your request, the changes in the Abstract is printed in accordance with the record.

In view of the foregoing your request in the matter is hereby denied.

A certificate of correction will issue for the remaining errors noted in your request.

Relief may be sought by submitting a fee of $100.

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For Cecelia B. Newman, Supervisor
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